What is claimed are:

1. A row decoder in a flash memory, comprising:

a PMOS transistor having a gate electrode for receiving a first input signal as an input and connected between a first power supply terminal and a first node;

a first NMOS transistor having a gate electrode for receiving the first input signal as an input and connected between the first node and a second node;

a second NMOS transistor having a gate electrode for receiving the second input signal as an input and connected between the second node and a ground terminal; and

a switching means having a gate electrode for receiving the third input signal as an input and connected between the second node and a second power supply terminal,

wherein the first node is connected to word lines.

2. The row decoder in the flash memory as claimed in claim 1, wherein a voltage outputted from the first power supply terminal is a positive voltage.

3. The row decoder in the flash memory as claimed in claim 1, wherein a voltage outputted from the second power supply terminal is a negative voltage.

4. The row decoder in the flash memory as claimed in claim 1, wherein the switching means consists of an NMOS transistor.

5. An erasing method in a flash memory cell using a row decoder, being characterized in that:

a word line to which a cell where a fail bit occurred is connected and a word line to which a cell where the fail bit did not occur is connected are discriminated, and

in an erasing mode, in order to prevent insulation break of a dielectric film between a floating gate and a control gate in the cell where the fail bit occurred, a ground voltage is applied to the word line to which the cell where the fail bit occurred connected and a negative voltage being an erasing voltage is applied to the word line to which the cell where the fail bit did not occur is connected.

6. The erasing method in the flash memory cell as claimed in claim 5, wherein in the erasing mode, the row decoder is used in order to apply the erasing voltage to the word line, and wherein the row decoder comprises:

a PMOS transistor having a gate electrode for receiving a first input signal as an input and connected between a first power supply terminal and a first node;

a first NMOS transistor having a gate electrode for receiving the first input signal as an input and connected between the first node and a second node;

a second NMOS transistor having a gate electrode for receiving the second input signal as an input and connected between the second node and a ground terminal; and

a switching transistor having a gate electrode for receiving the third input signal as an input and connected between the second node and a second power supply terminal,

wherein the first node is connected to word lines.

7. The erasing method in the flash memory cell as claimed in claim 6, wherein in order to apply the ground voltage to the word line connected to the cell in which the fail bit occurred, a power supply voltage is applied as the first input signal and the second input signal and the negative voltage is applied as the third input signal, in order to apply the negative voltage being an erasing voltage to the word line connected to the cell in which the fail bit did not occur, the power supply voltage is applied as the first input signal and the third input signal and a negative voltage is applied as the second input signal, and the second power supply terminal outputs the erasing voltage.

8. The erasing method in the flash memory cell as claimed in claim 7, wherein in order to apply the ground voltage to the word line to which the cell where the fail bit occurred is connected, a voltage of about –8V is applied as the third input signal, in order to apply the negative voltage being the erasing voltage to the word line to which the cell where the fail bit did not

occur is connected, a voltage of about –8V is applied as the second input signal, and the erasing voltage is about -8V.

9. The erasing method in the flash memory cell as claimed in claim 5, wherein the flash memory cell comprises:

a tunnel oxide film formed on a semiconductor substrate;

a floating gate formed on the tunnel oxide film;

a dielectric film formed on the floating gate;

a control gate formed on the dielectric film; and

a source region and a drain region formed in the semiconductor substrate at both sides of the tunnel oxide film,

wherein the control gate is connected to the word line, and in the erasing mode, the semiconductor substrate applies the positive voltage, and the source region and the drain region are floated.

10. The erasing method in the flash memory cell as claimed in claim 9, wherein the voltage applied to the semiconductor substrate in the erasing mode is about +8V.

11. The erasing method in the flash memory cell as claimed in claim 5, wherein the cell where the fail bit occurred is one in which the floating gate and the source/drain contacts are electrically connected to represent a low trans-conductance characteristic.